NOSSDAV 2002

The 12th International Workshop on Network and Operating Systems Support for Digital Audio and Video

Call for Papers
Organizing Committee
Local Information
Paper Submission
Conference Program
Registration

May 12-14, 2002
Wyndham Hotel, Miami Beach, FL, USA

WELCOME TO NOSSDAV 2002!

The NOSSDAV organizing committee invites you to attend this year's conference, which will be held at the Wyndham Hotel in Miami Beach, Florida, May 12-14 2002.

For 11 years, NOSSDAV has been an outstanding forum for researchers and developers involved in building innovative multimedia systems, networks, and applications. NOSSDAV brings together researchers, developers, and practitioners from academia and industry to present and discuss new ideas and future directions in networking and operating systems support for multimedia. NOSSDAV 2002 is sponsored by the Special Interest Group on Multimedia (ACM SIGMM) of the Association for Computing Machinery (ACM).

The Latest News

- NOSSDAV 2002 is in conjuction with IWQoS
- The conference program is now available
- Hotel and Registration are now available

Important dates

Workshop:	May 12-14, 2002
Early Registration Deadline	April 11, 2002
Camera Ready Deadline:	April 5, 2002
Acceptance Notification:	March 4, 2002
Submission Deadline (extended):	January 18, 2002 (midnight PST)

Sponsored by: ACM SIGMM Microsoft Research

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Registration Information

Early Registration Deadline: April 11, 2002

Registration Fees*	On or Before April 11, 2002	After April 11, 2002
ACM Member	$400	$450
Non-ACM Member	$450	$500
Student	$300	$350

*Registration fee includes admission to the workshop, copy of proceedings, continental breakfasts, lunches, coffee breaks, and the social event.

Cancelation Policy:

Written requests for refunds must be received no later than April 11, 2002. Refunds are subject to a $50 processing fee. All no-show registrations will be billed in full.

Registration:

Early registration is closed. On-site registration will be available on Sunday May 12, 5:00PM-8:00PM, and Monday May 13, 8:00AM - 10:00AM.

For further information please contact the program chairs Kevin Almeroth and James Griffioen.

Conference Program

All workshop sessions are held in the Regency Ballroom

May 12, 2002

5:00 PM - 8:00 PM	Registration, continues at 8:00 AM - 10:00 AM on May 13 (Mezzanine Foyer)

May 13, 2002

8:00 AM - 9:00 AM	Contentinal Breakfast
9:00 AM - 10:30 AM	Keynote Address: *Programmable Network Processors -- an opportunity for proactive networking* [abstract] Alan Crouch, Intel Corporation
10:30 AM - 11:00 AM	Break
11:00 AM - 12:30 PM	Network Issues for Video and Games Session Chair: Christos Papadopoulos, USC *Adaptive Rate Control for Streaming Stored Fine-Grained Scalable Video* Philippe de Cuetos, Keith W. Ross *Probabilistic Congestion Control for Non-Adaptable Flows* Joerg Widmer, Martin Mauve, Jan Peter Damm *On the Impact of Delay on Real-Time Multiplayer Games* Lothar Pantel, Lars C. Wolf
12:30 AM - 1:30 PM	LUNCH (Lobby Lounge)
1:30 PM - 2:30 PM	Potporri Session Chair: Christophe Diot, Sprint ATL *Characterizing Locality, Evolution, and Life Span of Accesses in Enterprise Media Server Workloads* Lucy Cherkasova, Minaxi Gupta *The Design of a Transport Protocol for On-Demand Graphical Rendering* Albert Harris, Robin Kravets
2:30 PM - 3:00 PM	Break
3:00 PM - 4:30 PM	VoIP Session Chair: Venkata Padmanabhan, Microsoft *SIP-based Conference Control Framework*

	Petri Koskelainen, Henning Schulzrinne, Xiaotao Wu *Impact of Link Failures on VoIP Performance* Catherine Boutremans, Gianluca Iannaccone, Christophe Diot *Comparison and Optimization of Packet Loss Repair Methods on VoIP Perceived Quality under Bursty Loss* Wenyu Jiang, Henning Schulzrinne

May 14, 2002

8:00 AM - 9:00 AM	Contentinal Breakfast
9:00 AM - 10:30 AM	Mobile and Wireless System Session Chair: Robin Kravets, UIUC *Understanding Bandwidth Allocation Techniques for the First-Hop in Wireless Networks* Lili Qiu, Victor Bahl, Atul Adya *Application Level Hand-off Support for Mobile Media Transcoding* Sessions Sumit Roy, Bo Shen, Vijay Sundaram, Raj Kumar *Integration of Dynamic Voltage Scaling and Soft Real-Time Scheduling for Open Mobile Systems* Wanghong Yuan, Klara Nahrstedt
10:30 AM - 11:00 AM	Break
11:00 AM - 12:00 PM	Distribution Overlays Session Chair: Dan Rubenstein, Columbia *Broadcast Federation: An Application-layer Broadcast Internetwork* Yatin Chawathe, Mukund Seshadri *Topology-Aware Overlay Networks for Group Communication* Minseok Kwon, Sonia Fahmy
12:00 PM - 1:00 PM	LUNCH (Lobby Lounge)
1:00 PM - 2:30 PM	Video Streaming I Session Chair: Su Wen, Univ of Kentucky *A Demand Adaptive and Locality Aware (DALA) Streaming Media Server Cluster Architecture* Zihui Ge, Ping Ji, Prashant Shenoy *Optimal Proxy Management for Multimedia Streaming in Content Distribution Networks* Chitra Venkatramani, Olivier Verscheure, Pascal Frossard, Kang-Won Lee *Selecting among Replicated Batching Video-on-Demand Servers* Meng Guo, Mostafa Ammar, Ellen Zegura

2:30 PM - 3:00 PM	Break
3:00 PM - 4:00 PM	Video Streaming II Session Chair: Kevin Almeroth, UCSB *A Framework for Scalable and Inexpensive Video Delivery* Min-You Wu, Su-Jun Ma, and Wei Shu *Distributing Streaming Media Content Using Cooperative Networking* Venkata N. Padmanabhan, Helen J. Wang, Philip A. Chou, and Kunwadee Sripanidkulchai

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Location:

Wyndham Miami Beach Resort
4833 Collins Avenue
Miami Beach, Florida.

Hotel Rates:

- Single/Double Occupancy: $139/night
- Triple Occupancy: $149/night
- Quad Occupancy: $159/night

(Note: If you bring a car, there is a $18 per night parking charge.)

Reservation Instructions:

- The cut off date for making a reservation at the conference rate is April 11, 2002.
- Please call 1-800-20-EVENT to make reservations. Mention the block code "ACM/NOSSDAV" to get the conference rate.

Transportation:

Miami International Airport is located about 12 miles/15km (about 20 minutes) from the Wyndham Miami Beach Resort.

- Taxis: The fare from the airport to the Miami Beach Ocean resort is approx. $25.00. From the hotel to downtown it is approx. $15-$18.
- Commercial Shuttles: Super Shuttle (door-to-door airport service). Approx. $13 per person. 305-871-2000.
- Public Transportation: Metro buses run to downtown, North Miami Beach, Coral Gables and Hialeah. Fare is US$1.25, exact change required; no real room for luggage. 305-770-3131.

Other Local Information:

Dining Leisure Activities Arts and Culture Events Shopping

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NOSSDAV paper submission

NOSSDAV only reviews and publishes original work not currently under consideration elsewhere, as described below. Papers not meeting these criteria will be withdrawn from the conference without review as soon as the conflict comes to the attention of the program committee.

Papers must be submitted electronically in the manner and format detailed below. Authors for whom this presents a severe problem should contact one of the technical program committee co-chairs to discuss alternatives.
The submission deadline is Jan. 18, 2002 (midnight PST).

Papers must be formatted according to the IEEE or ACM standard double-column format. We suggest the use of 11pt font size.

LaTeX, Framemaker and Microsoft Word files cannot be accepted. **You must submit PDF or PostScript**.

Papers with more than 5 pages will not be reviewed.

To register and submit a paper, please go to the electronic submissions page.

Dual Submission Policy

It is in the interest of NOSSDAV and its attendees that material presented at NOSSDAV has not been published elsewhere. Also, reviewing the same material twice wastes scarce reviewer resources. Waiting for NOSSDAV reviews can significantly improve a potential journal submission and avoids that two different sets of reviewers make similar recommendations.

Given these motivations, the following policies hold:

- Once submitted to NOSSDAV, a paper cannot be submitted to another workshop, conference or journal until the NOSSDAV acceptance decision is known.
- A paper that is under consideration elsewhere, including a workshop or journal, cannot be submitted to NOSSDAV.
- If material has appeared or is likely to appear in a workshop, the paper should indicate so. This is only acceptable if the NOSSDAV paper provides substantial additional results compared to the earlier or pending publication or if the workshop produced no printed proceedings.

Programmable Network Processors -- an opportunity for proactive networking

Alan Crouch
Director, Network Platforms
Intel Labs
alan.crouch@intel.com
May 13, 2002

NOSSDAV **2002**

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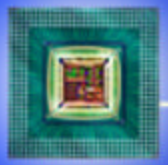
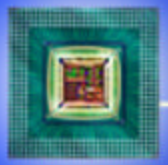


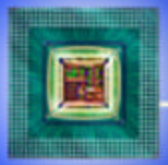
OUTLINE

- The Environment
- What is a network processor?
- Intel's Vision and Contribution
- Technical Challenges
- Summary

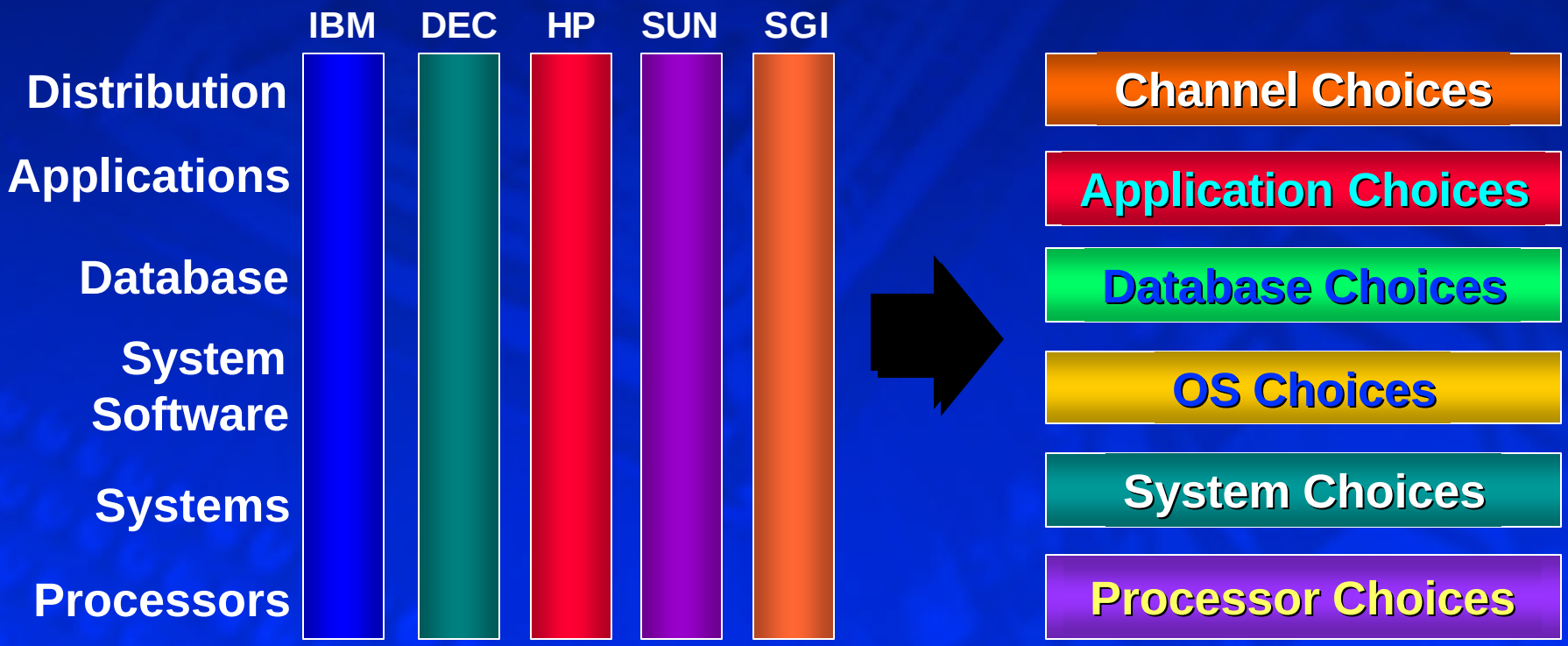


Communications Industry Transition

- **Vertically integrated communication vendors moving to building block approach**
  - **Programmable switching platform**
  - **Control/Service logic moves to standard computing platforms**
- **Implications**
  - **Multiple, independent services on same switching platform**
  - **Allows rapid, dynamic innovation in services**
  - **Customer, service or VPN-specific resource guarantees possible**
  - **Example: SoftSwitch Initiative**



Lesson from the past: Computer Industry Transition

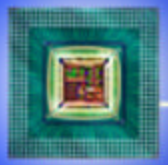


"Old Computer Industry"

"New Computer Industry"

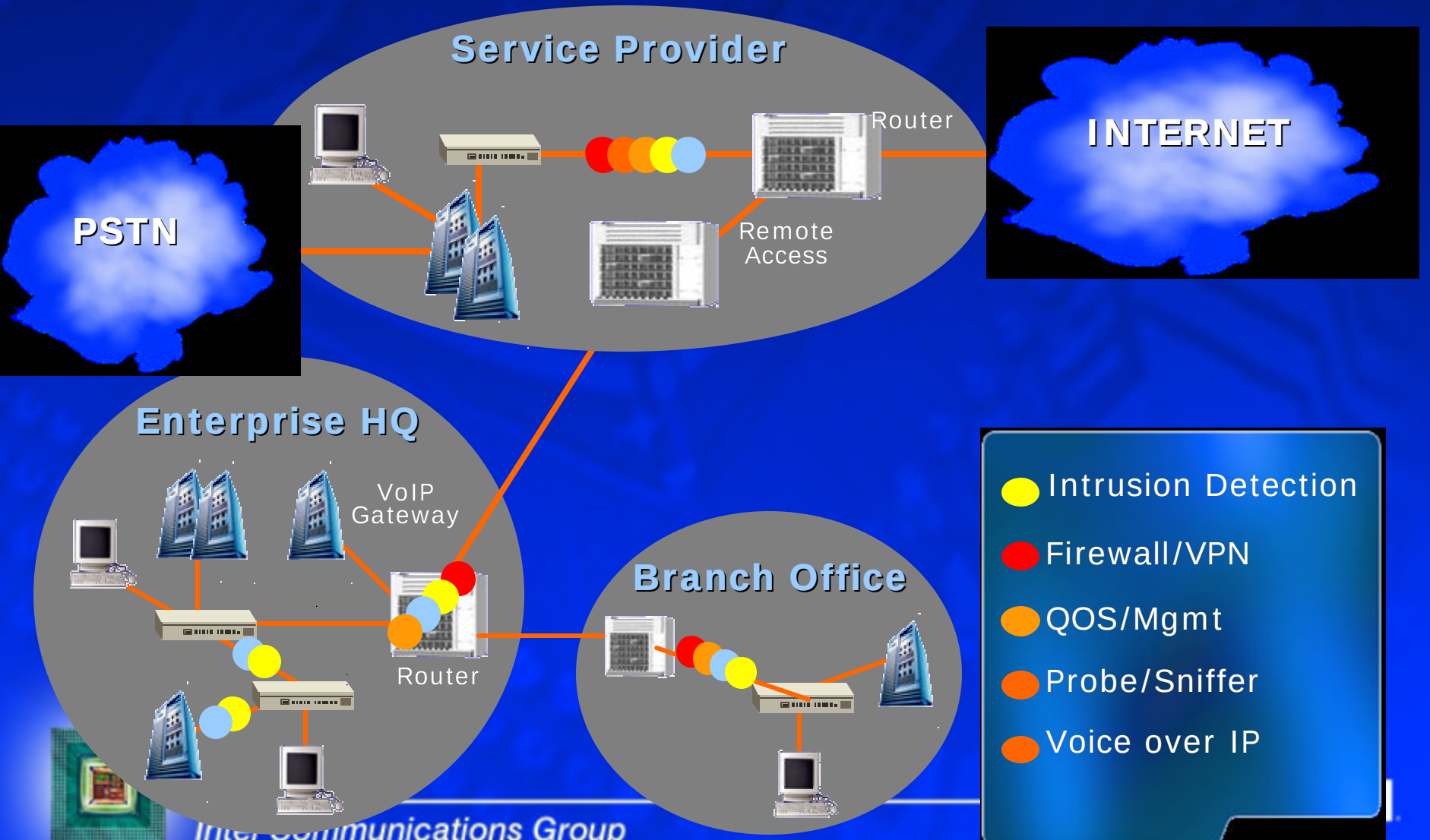
Business Value Proposition for Systems Vendors

- ASICs giving way to programmable Silicon
  - Time-to-Market, Price/performance, Flexibility reasons
  - Efficient suppliers: IBM, AMCC, Intel, Motorola, …
- Value moving to services and applications
  - L3/L4 switches already a commodity
  - End2End services require integration across multiple technologies and infrastructures
  - Service providers want quick ways of deploying new services
- New services via middleware infrastructure
  - E.g., policy, security infrastructure, directories, JAVA*/JINI*, CORBA*/DCOM*, …



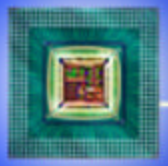
*Other names and brands may be claimed as the property of others

Where Network Services Live or “edge” is everywhere



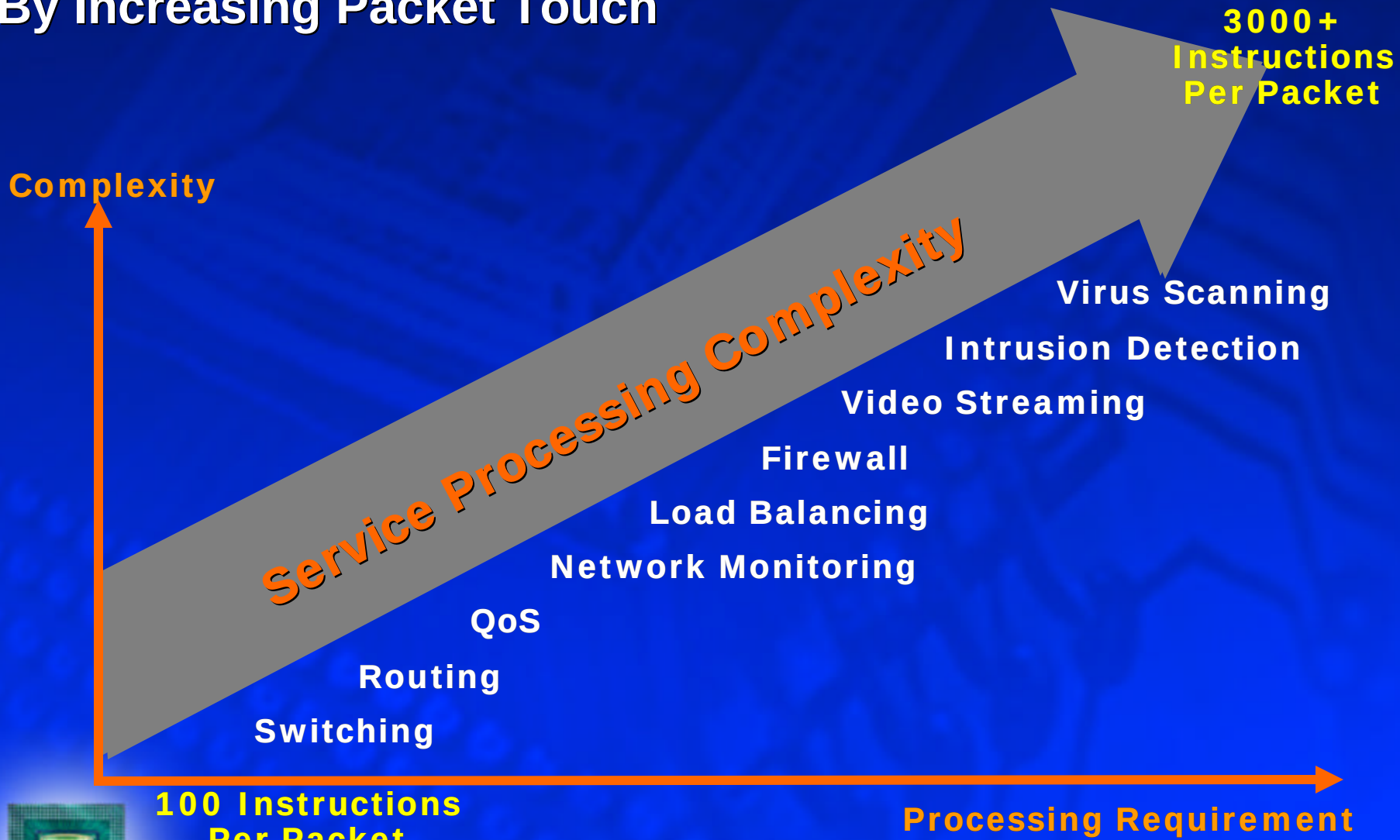
Changing notion of “network edge”

- New services deployed throughout the nodes of the network
  - VPNs, intrusion detection
  - QoS-enabled Video streaming and distribution
- Edge services require:
  - More per-packet processing
  - Flexibility to upgrade nodes in the field
- IP-based networks are no longer passive packet forwarders
  - Must proactively respond to network dynamics to ensure high-availability and security.



Services Increase the Processing Load

By Increasing Packet Touch

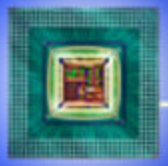


More Detailed Categorization of Service Processing Requirements

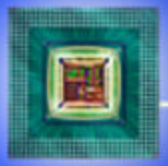
- ***The characterization is really multi-dimensional (still simplified):***

Service	Data touch	State touch	Compute Requirements
Switching	Low	Low/Med	Low/Med
Routing	Low	Low/Med	Low/Med
QoS	Low/Med	Low/Med	Low/Med
Stateful Firewall	Low/med	Low/Med	Low-High
Proxy Firewall	Med/high	Med	Med
Load Balancing	Med	Med/High	Low/Med
CB Load Balance	High	Med/High	Low/Med
VPN	High	Med	High
Virus Detection	High	High	High
IDS	High	High	High

* Crypto processing needs a special processor.



Network processors to the rescue ….



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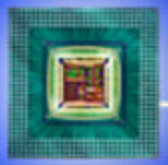
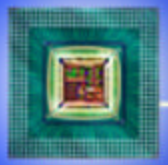


What is a Network Processor (NPU)?

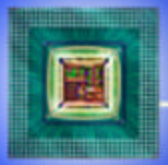
- **Flexible Programming Capability**
  - Programmability, with rich packet processing features
- **Capable of L2-L4+ data processing at wire rates**
- **Highly integrated Processor**
  - Microcoded and/or hardwired acceleration engines
  - Memory subsystem controller(s)
  - Closely coupled with media (integrated or attached)
  - Good data flow management, internal comm's support, and partitioning to enable acceleration
  - Memory latency hiding techniques includes memory controllers

Highly integrated compute, memory and media resources to tackle packet processing problems close to the wire.



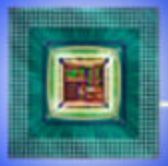
Problem Spaces Targeted by NP's

- CPE, Edge/Access, and Core applications
  - Encapsulation/Decapsulation to fabric/backplane
  - Switching/Routing (L2/L3/L4)
  - Cell/packet conversion
- L4-L7 applications; content and/or flow-based
- Intrusion Detection (IDS) and Proactive monitoring of networks
  - Particularly challenging
  - needs processing of many state elements in parallel,
    - unlike most other networking apps which are more single-path per packet/cell



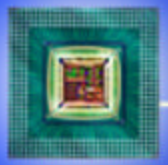
Why not just use a GHz+ Pentium?

- Network processing is basically a dataflow problem
  - Almost every new packet requires new state
  - uP caches do not hide latency
- Time budgets per cell/packet at high wire speeds are low
  - OC-48 arrival rate = 160ns, OC-192 arrival rate = 35ns, OC-768 arrival rate = 8ns



NPUs can provide acceleration

- Keep stalls on memory and cache to a minimum, and provide specialized compute capabilities
- Offload high-touch portions of applications
  - Header parsing, checksums/CRCs, RegEx string search
- Offload latency-intensive portions to reduce stall time
  - pointer-chasing in hash table lookups, fetch of candidate portion of packet for header parsing
- Offload compute-intensive portions with specialized engines
  - Crypto computation, ATM CRC, packet classification
- Provide efficient system management
  - Buffer management, descriptor management, communications among units, timers, queues, etc.



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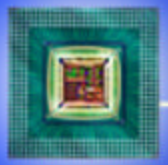
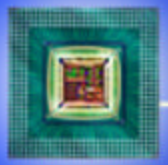


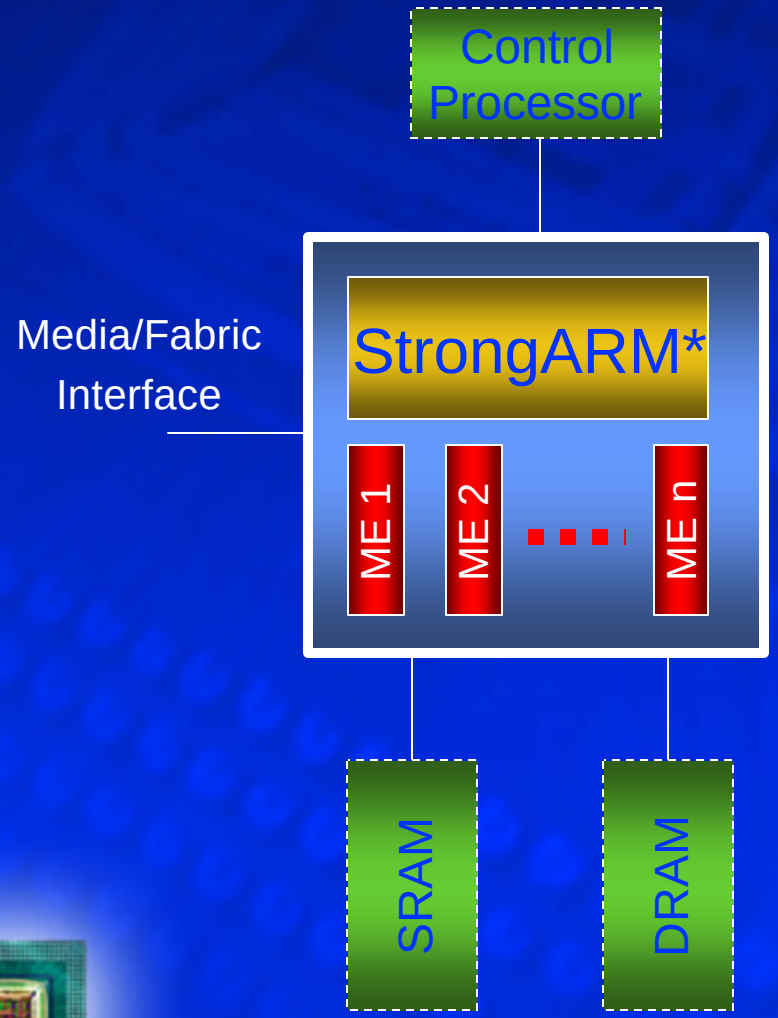
Intel Vision: rich offering of modular networking building blocks

Key Industry Transitions

- Ethernet
  - 10G emergence in metro
  - Provide building blocks at every level
    - Optics, framers, network processors, switch fabrics
- Processing in the Network
  - IXP family of network processors
- End2End view
  - Clients (LAN, wireless, cable modem, xDSL, etc)
  - Enterprise (SAN, switch fabrics)
  - Metro/Core
    - Building blocks for access/edge and core routers



IXP Network Processors



- **Microengines**
  - **RISC processors optimized for packet processing**
  - **Hardware support for multi-threading**
- **Embedded StrongARM/Xscale™**
  - **Runs embedded OS and handles exception tasks**

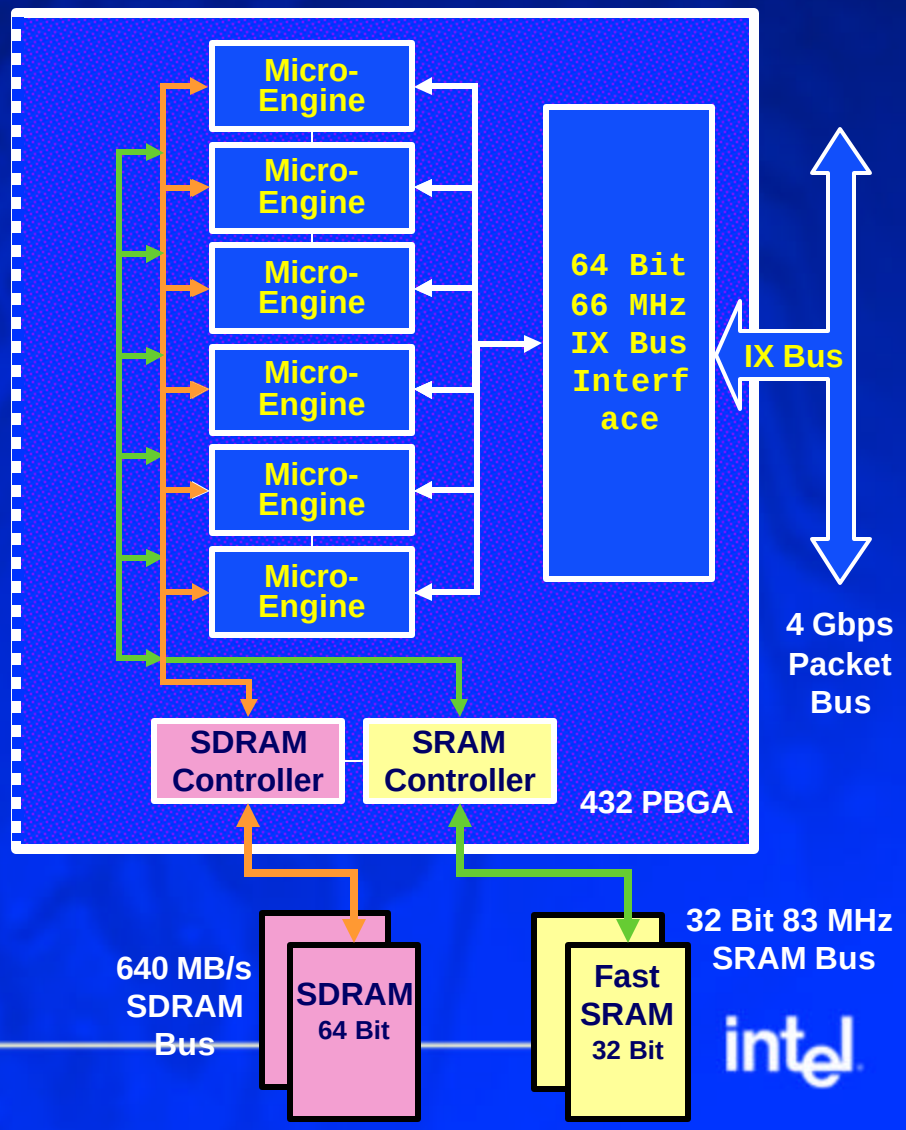
*Other names and brands may be claimed as the property of others

IXP Network Processor Family - Multi-Processor Architecture

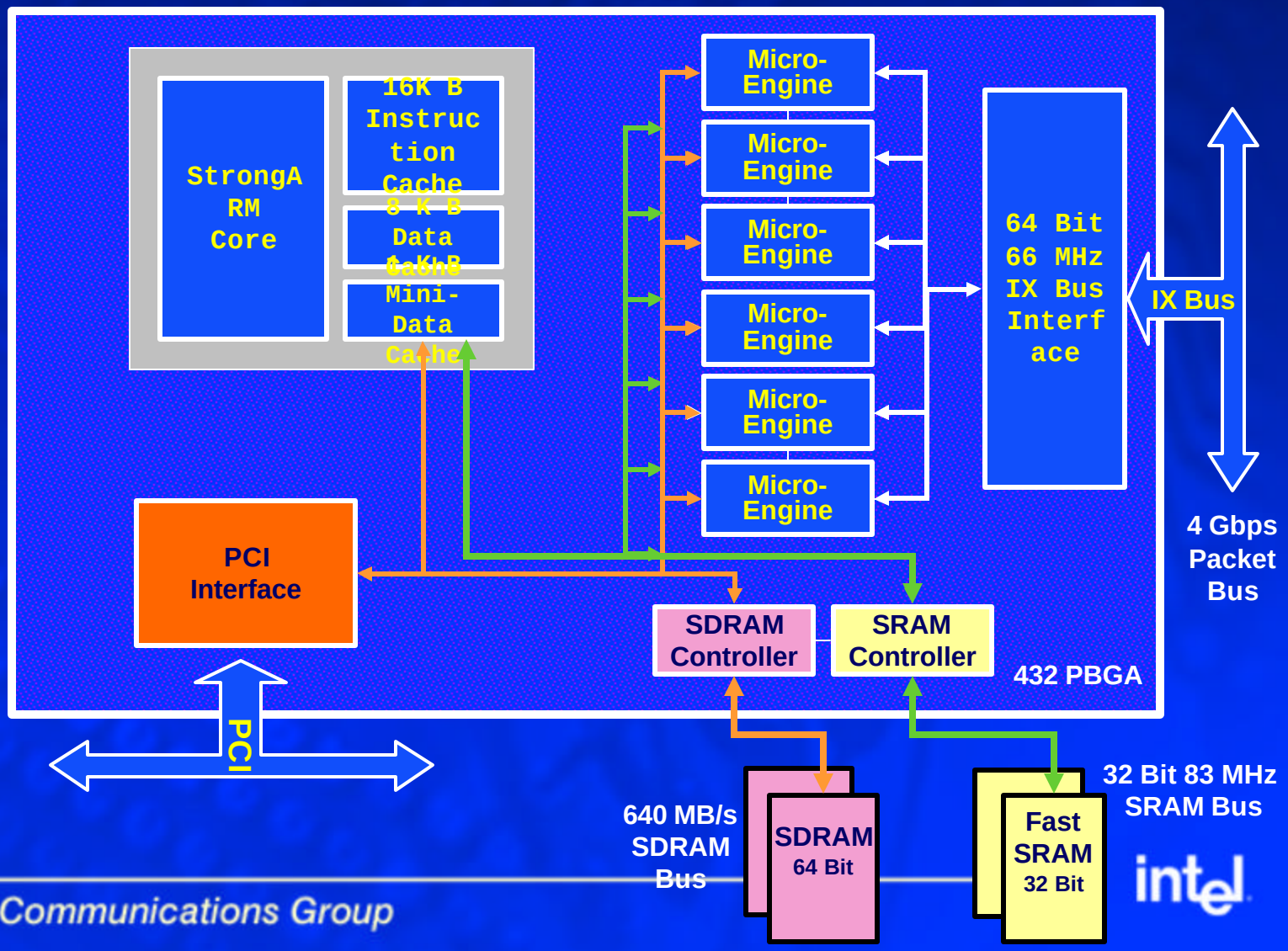
Parallel Micro-Engines

- Programmable 32-Bit RISC Processors (232 MHz->1.4GHz)
  - Independent Control Store
  - Local I/O Transfer Store
- Equal access to all resources
  - SRAM & SDRAM Memory
  - IX Bus & PCI Peripherals
- Non-Blocking Internal Buses
  - > 2X External Bandwidth
  - Eases programming

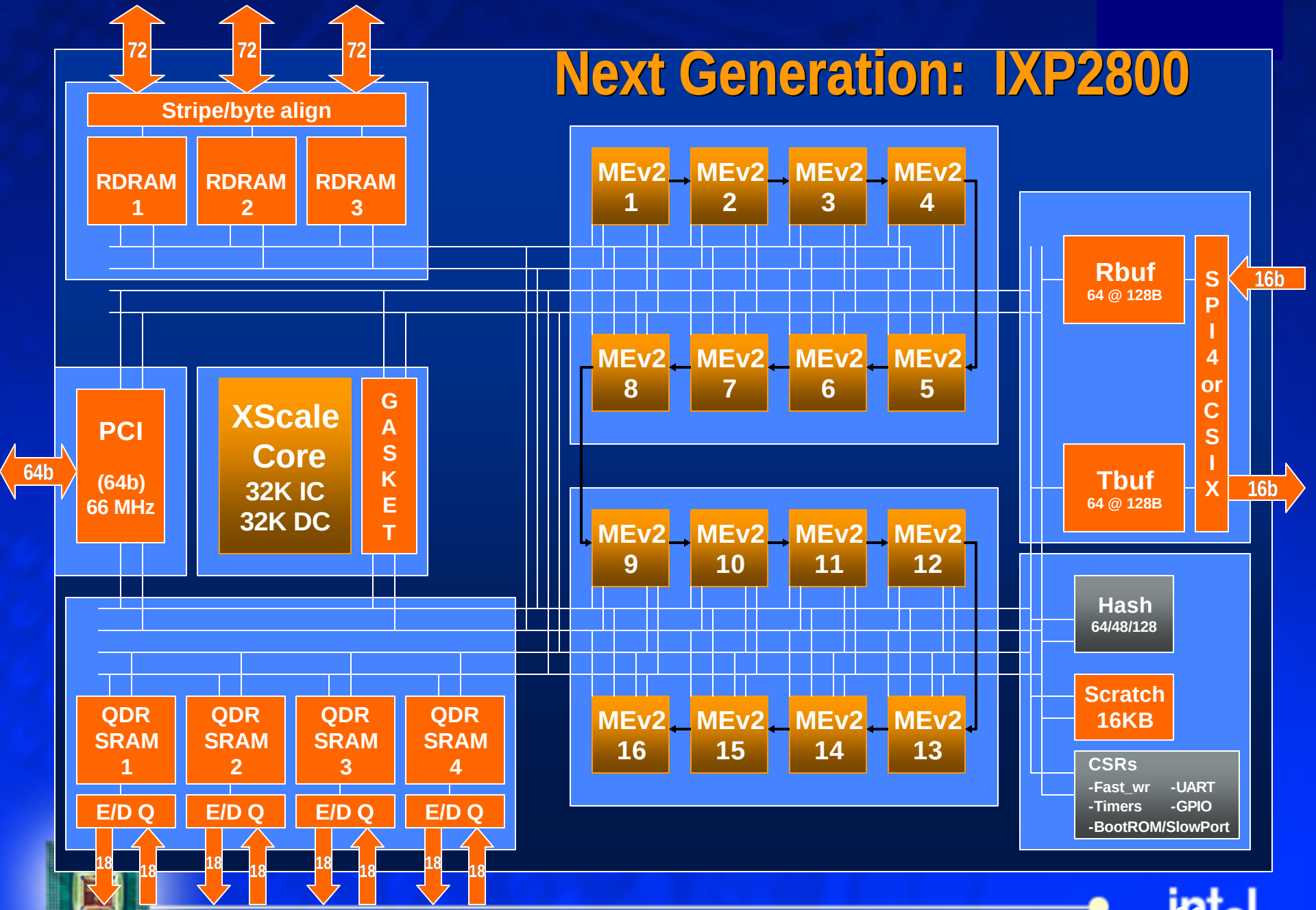
Parallel Operation Supports Very High Throughput



Current Offering: IXP12xx Network Processor

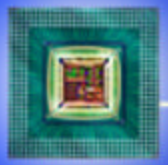


Next Generation: IXP2800



2nd Generation Hardware Features: *Performance and Ease of Programming with a Mixed Pipeline*

- **Ring Buffers**
  - Allows for Context and Functional Pipeline to talk to each other without horrendous synchronous timing issues
  - Use the best type of pipeline for the job
- **Next Neighbor Registers and Signaling**
  - Allows for single cycle transfer of context to the next logical micro-engine to dramatically improve performance
  - Simple, easy transfer of state
- **Distributed data caching within each micro-engine**
  - Allows for all threads to keep processing even when multiple threads are accessing the same data
- **1.4Ghz initial micro-engine clock speed**
  - Speed is good!

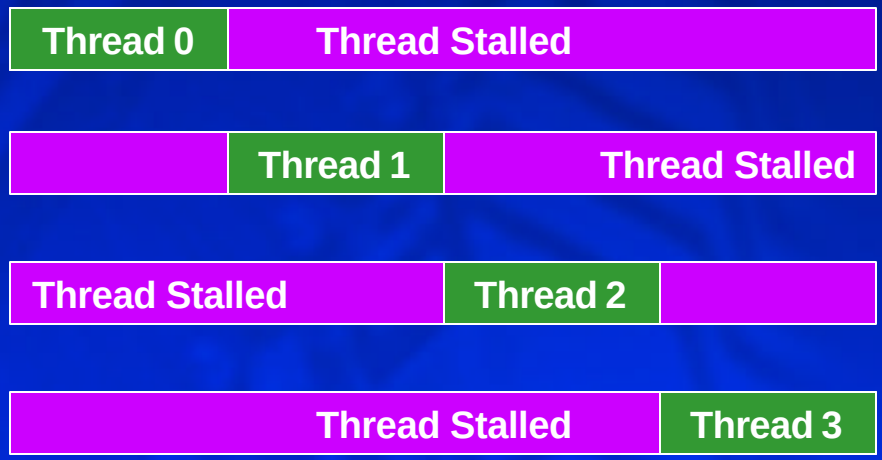


intel

Why Hardware Multi-Threading?

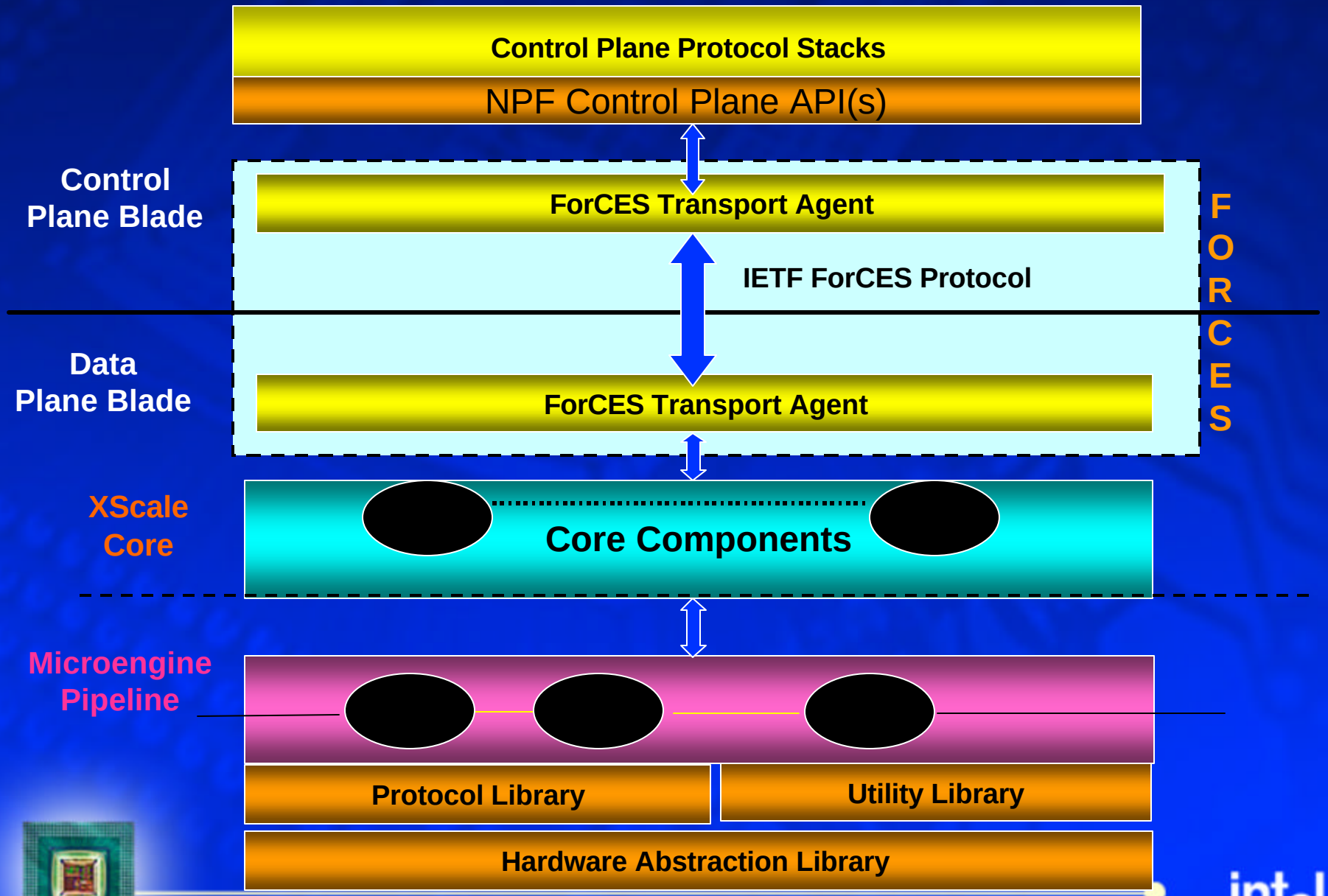
- Ensures efficient use of micro-engine pipeline
  - Simulation results indicate ~75% of cycles spent waiting for memory
- If single threaded, the equivalent performance would require 24 engines
  - Huge silicon savings
- Keeps micro-engine pipeline active during otherwise idle periods due to memory latency

Four Threads Executing on a Single Microengine

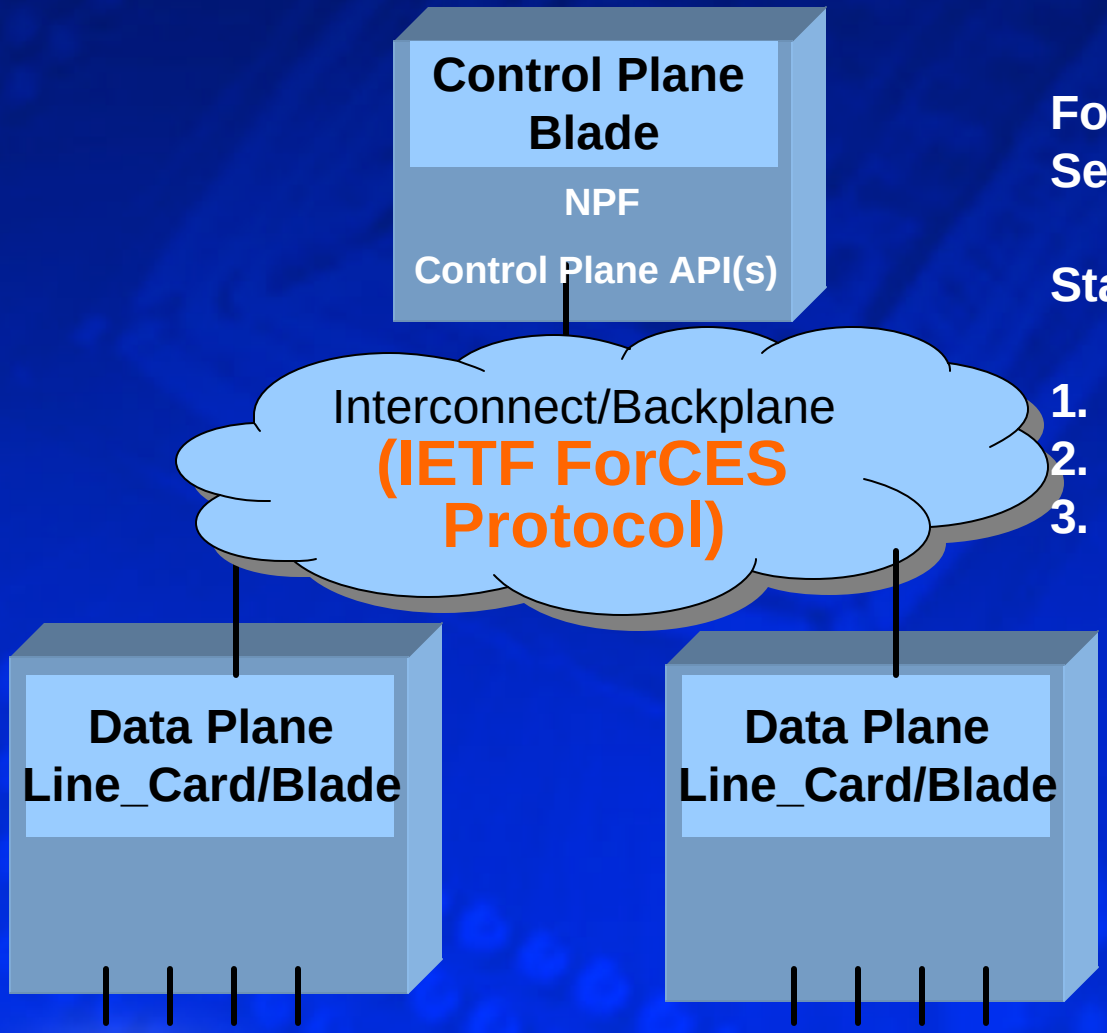


Going to 16 engines, 8 Threads each in IXP2800 (128 HW threads!)

IXA Portability Framework



What is IETF ForCES?



Forwarding and Control Element Separation for IP Networks

Standards track work in three steps (expected milestones):

1. **Internet draft -- current**
2. **Draft standard – 2002/early 2003**
3. **Standard – late 2003**

Join us: www.sstanamera.com/~forces

Next IETF meeting: July 14-19, Yokahama, Japan

IXA University Program

- Enable universities around the world to incorporate IXA-based components into research and curriculums:
- Three primary goals:
  1. Encourage the use of the IXA in both research and curriculum.
  2. Create a community of IXA-related research universities
  3. Give students the hands-on experience and training in building and experimenting with real-world network applications using IXA.

For More Information:

www.intel.com/research/university/comm/index.htm

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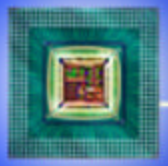
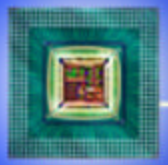
- Technical Challenges
- Summary



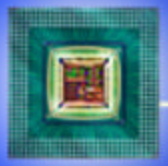
Programmability brings flexibility and potential for change

- Migrating Internet to a robust infrastructure when ….
  - Fragile and vulnerable IP networks vs. robust voice networks
  - Inflexible ASICs have limited capabilities in the fast path with little insight into network health
  - Only insufficient, stale & unreliable statistics provided through old SNMP MIB-II & RMON polling-based mechanisms
- … The world is moving
  - DoS and DDoS Attacks are on the rise
  - Network worms are devastating networks (eg. Code Red)
  - Highly transactional mission critical applications demand robust networks
  - Streaming applications, SLAs and QoS
  - Dynamic Traffic Engineering



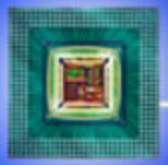
Example Opportunity

- **Programmable NPUs for advanced video streaming platforms**
  - **Handle a variety of streams**
  - **QoS and Quality adaptation over mobile and wireless**
  - **Efficient overlays to achieve multipoint streaming independent of underlying infrastructure**
  - **Dynamic adaptation to attacks, failures**



How Network processors can help

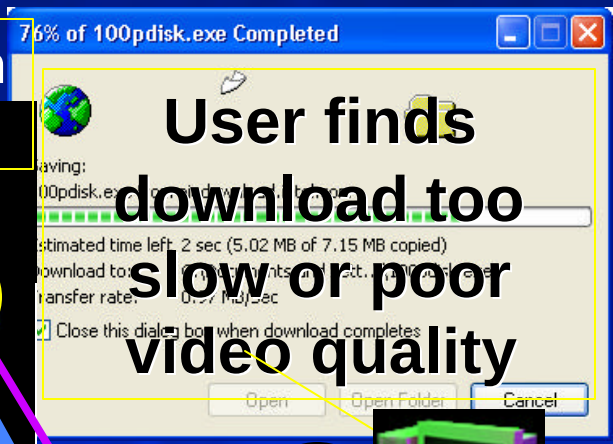
- **Programmable and secure infrastructure**
  - **Robust, verifiable code on the network nodes**
  - **Verifiable transactions among nodes**
  - ***Watchdog* and *bloodhound* nodes distributed in the infrastructure**
    - **A cooperative model based on information sharing**
    - **Watch for performance anomalies and trigger reactions**
      - Route changes, install new label-switched paths, etc
    - **Watch for behavior anomalies in traffic and nodes**
      - Squelch the traffic closer to the entry
      - “replace” misbehaving nodes with alternate paths



Example: Proactive, robust video streaming infrastructure

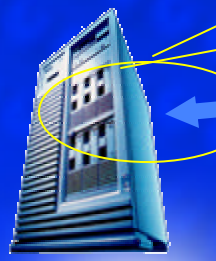
Traffic can be redirected across uncontested paths, or marked with high QoS

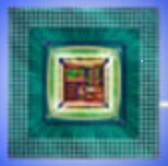
Service Verification E2E

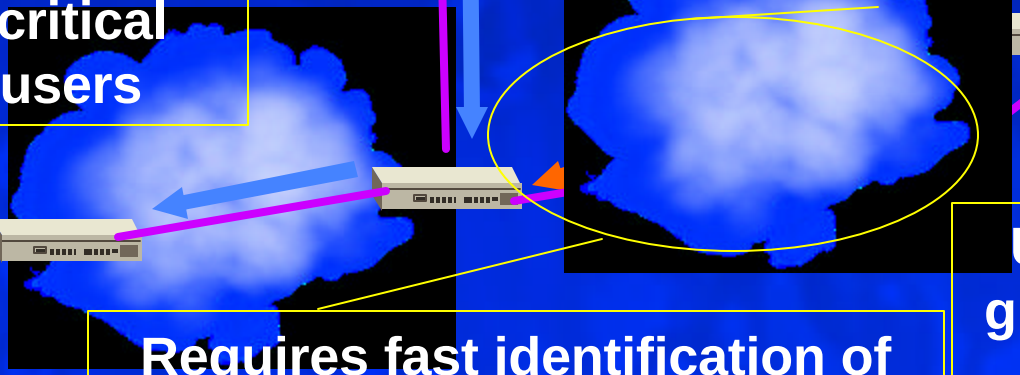


User finds download too slow or poor video quality

Web Server state distinguishes mission critical apps & users



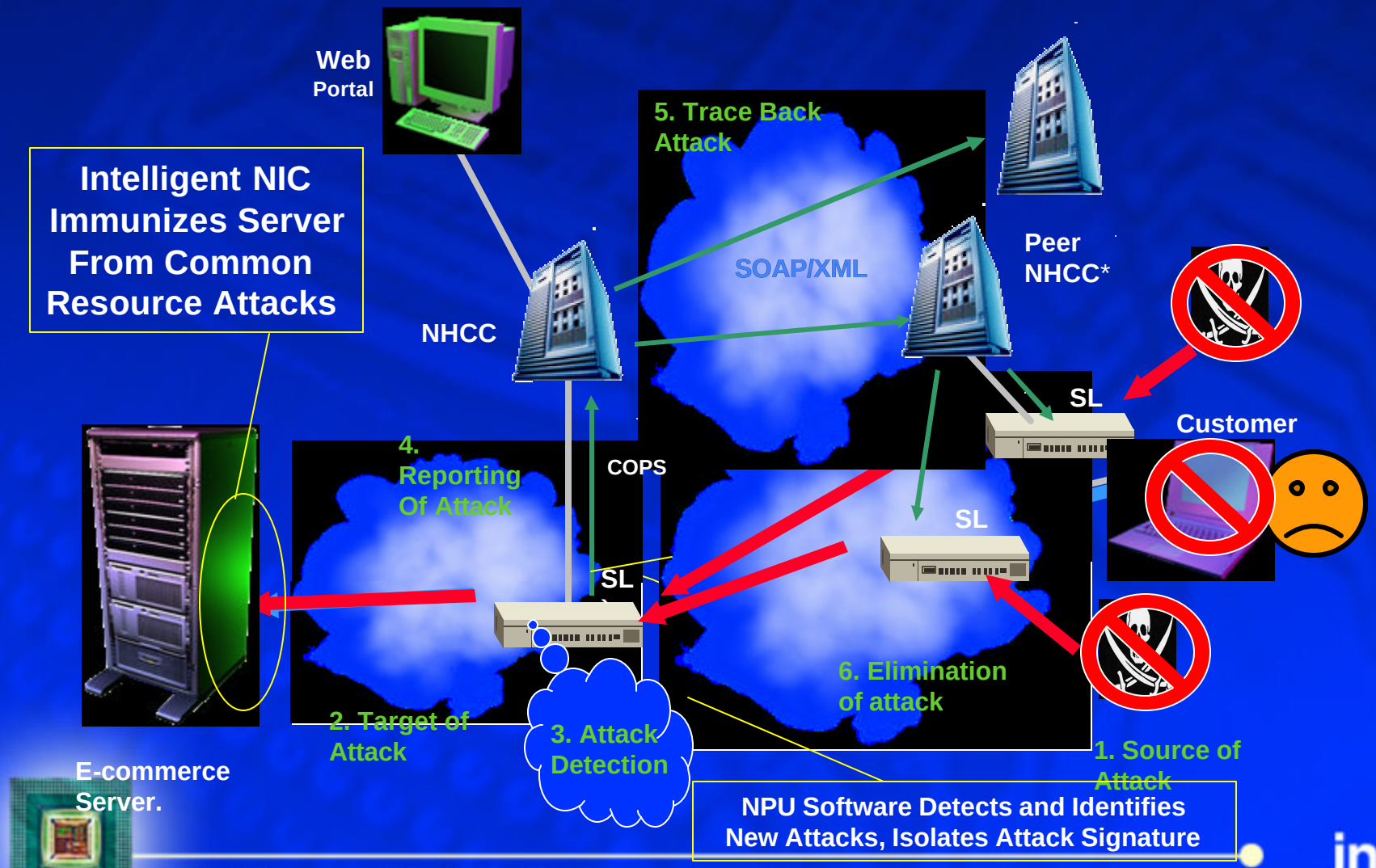




User gets instant gratification, with a fast download.

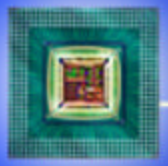
Requires fast identification of mission critical flows correlated with server state

Server Is Targeted for a Distributed TCP SYN Flood Attack



OUTLINE

- Overall Vision
- IXP Architecture
- Software Support
- Technical Challenges
- Summary



Summary

"Edge" is everywhere

- Services being deployed at all network nodes
- Dynamic/Rapid service deployment requires data-plane programmability

Network Processors evolving to meet the challenge

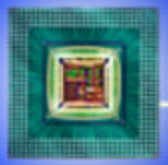
- Packet Processing: more instructions per packet
- Evolving functionality: Big advancements this year

Opportunity: Proactive Networks programmable platform

- Quality of Service, Media Processing, Anomoly Detection and Correction
- Rapid/Dynamic deployment: Add new functionality on the fly

Join us in Proactive Networks research efforts

www.intel.com/research/university/comm/index.htm



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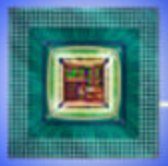
BACKUP



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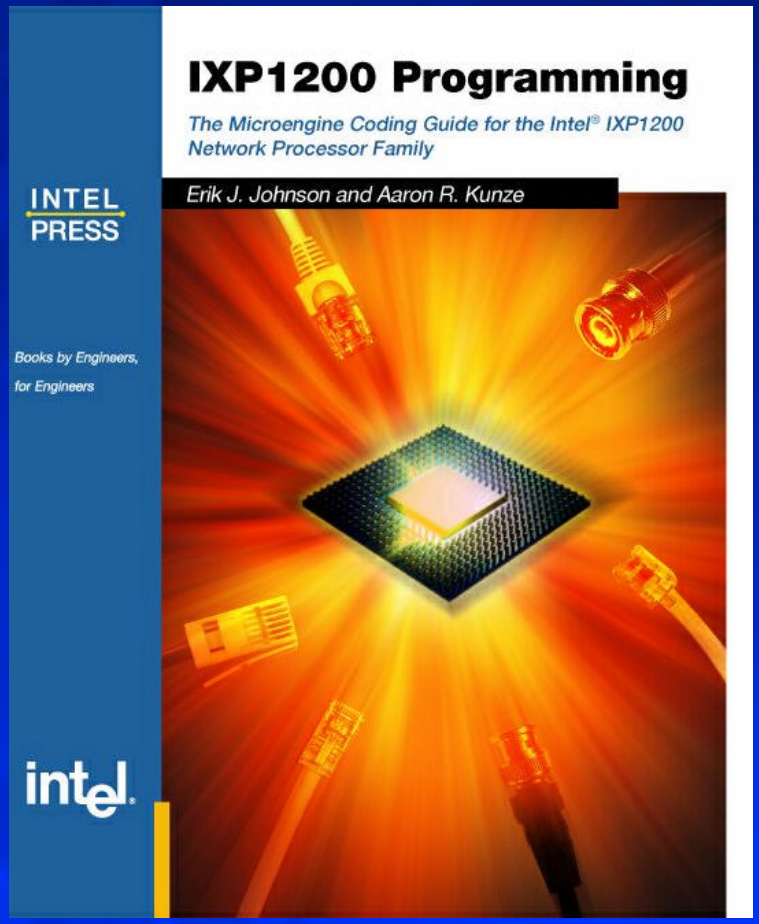

- **Topics include:**
  - **Microblocks and microACEs**
  - **Microengine C**
  - **Receiving, processing and transmitting packets**
  - **Data structure and algorithm design**

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Title:
Programmable Network Processors -- an opportunity for proactive networking

Speaker: Raj Yavatkar, Intel Corporation

Abstract:

With the rapid adoption of ubiquitous Internet access for e-business, mission-critical processes and operations are now moving to the Internet. More and more businesses use the Internet for supply chain management, customer service, and intra-enterprise operations. This movement has redefined the notion of the "network edge" by requiring almost every network node to deploy some or all of the sophisticated network services such as VPNs, intrusion detection, load balancing, and differentiated services. Such services require more per-packet processing and flexibility to upgrade functionality of nodes in the field. Moreover, the IP-based networks are no longer passive packet forwarders, but entities that must proactively respond to network dynamics to ensure high-availability and security.
This trend is accompanied by the commercially availability of network processors that offer an alternative to the fixed-function ASICs by providing programmability and flexibility. We will explore the concept of network processors (NPUs) and their impact on traditional networking. We will also describe the opportunities for advanced research in building proactive networks.